IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please cancel claims 3, 5, 12, 19, 25 and 39 and amend the following claims:

1. (Twice Amended) A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a pair of transistors [dual-gate transistor] of a second conductivity type coupled at a drain region and coupled at a source region, and wherein the [a] drain region for the pair of transistors [dual-gate transistor] in each inverter is coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to a gate of one of the pair of transistors in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a [first] gate of one of the pair of transistors [the dual-gate transistor] in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the pair of transistors [dual-gate transistor] and the drain region of the transistor of the first conductivity type in each inverter.

2. (Twice Amended) The sense amplifier of claim 1, wherein the transistor of a first conductivity type is a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the pair of transistors [dual-gate transistor] of a second conductivity type are [is an] n-channel metal oxide semiconductor (NMOS) transistors.

4. (Twice Amended) A sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a pair of [dual-gate] n-channel metal oxide semiconductor (NMOS) transistors coupled at a drain region and a source region, and wherein a drain region of the PMOS transistor in each inverter is coupled to the [a] drain region for the pair of NMOS transistors [dual gate NMOS transistor] in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to a gate of one of the pair of NMOS transistors in the other inverter of the pair of cross-couple inverters;

a bit line coupled to each inverter, wherein each bit line couples to a [first] gate of one of the pair of [the dual-gate] NMOS transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region for the PMOS and the [dual-gate] NMOS transistors in each inverter respectively.

10. (Twice Amended) A latch circuit, comprising:

a pair of cross-coupled amplifiers, wherein each amplifier includes:

a first transistor of a first conductivity type;

a second transistor and a third transistor [dual-gate transistor] of a second conductivity type, wherein the second and the third transistor in each amplifier are [a drain region for the dual-gate transistor in the inverter is] coupled at a drain region and are coupled at a source region, and wherein a [the] drain region for the second and the third transistors are [is] coupled to a drain region of the first transistor in the same amplifier, are coupled directly to a gate of the first transistor of the first conductivity type in the

other amplifier in the pair of cross-coupled amplifiers, and are coupled to a gate of the third transistor in the other amplifier in the pair of cross-coupled amplifiers;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to a [first] gate of the second transistor [dual-gate transistor] in each amplifier; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the first transistor and to the drain region of the second and the third [dual-gate] transistors.

11. (Twice Amended) The latch circuit of claim 10, wherein the first transistor includes a p-channel metal oxide semiconductor (PMOS) transistor, and wherein the second and the third [dual-gate] transistors include[s an] n-channel metal oxide semiconductor (NMOS) transistors.

17. (Once Amended) An amplifier circuit, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gated metal-oxide semiconducting field effect transistor (MOSFET) of a second conductivity type, wherein the transistor of a first conductivity type in each inverter and the a dual-gated MOSFET are coupled at a drain region in the same inverter, and wherein the drain region in each inverter is further coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gated MOSFET in the other inverter of the pair of cross-couple inverters;

a pair of input transmission lines, wherein each one of the pair of input transmission lines is coupled to another [first] gate of the dual-gated MOSFET in each inverter respectively; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region on each one of the pair of cross-coupled inverters.

23. (Twice Amended) A memory circuit, comprising:

a number of memory arrays;

at lease one sense amplifier, wherein the sense amplifier includes:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS) transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor

wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region of for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in the number of memory arrays, and wherein each one of the complementary pair of bit lines couples to a [first] gate of the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

29. (Twice Amended) An electronic system, comprising:

a processor;

a memory device; and

a bus coupling the processor and the memory device, the memory device further including a sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a p-channel metal oxide semiconductor (PMOS)

transistor; and

a dual-gate metal oxide semiconductor (NMOS) transistor wherein a drain region of the PMOS transistor in each inverter is coupled to a drain region for the dual-gate NMOS transistor in the same inverter, is coupled directly to a gate of the PMOS transistor in the other inverter of the pair of cross-couple inverters, and is coupled to one gate of the dual-gate NMOS transistor in the other inverter of the pair of cross-couple inverters;

a complementary pair of bit lines coupling the at least one sense amplifier to a number of memory cells in a memory cell array, and wherein each one of the complementary pair of bit lines couples to a [first] gate of the dual-gate NMOS transistor in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the PMOS transistor and the drain region for the dual-gate NMOS transistor in each inverter.

32. (Twice Amended) An integrated circuit, comprising:

a processor;

a memory operatively coupled to the processor; and

wherein the processor and memory are formed on the same semiconductor substrate and the integrated circuit includes at least one sense amplifier, comprising:

a pair of cross-coupled inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor in each inverter is

coupled to a drain region of the transistor of the first conductivity type in the same inverter, is coupled directly to a gate of the transistor of the first conductivity type in the other inverter of the pair of cross-couple inverters, and to one gate of the dual-gate transistor in the other inverter of the pair of cross-couple inverters;

a pair of bit lines, wherein each one of the pair of bit lines is coupled to a [first] gate of the dual-gate transistors in each inverter; and

a pair of output transmission lines, wherein each one of the pair of output transmission lines is coupled to the drain region of the dual-gate transistor and the drain region of the transistor of the first conductivity type in each inverter.

33. (Twice Amended) A method for forming a current sense amplifier, comprising:

cross coupling a pair of inverters, wherein each inverter includes:

a transistor of a first conductivity type;

a dual-gate transistor of a second conductivity type wherein a drain region for the dual-gate transistor is coupled to a drain region of the transistor of the first conductivity type; and

wherein cross coupling the pair of inverters includes directly coupling the drain region for the transistor of the first conductivity type and the drain region for the dual-gate transistor in one inverter to a gate of the transistor of a first conductivity type and to one [a second] gate of the dual-gate transistor in the other inverter.

35. (Twice Amended) The method of claim 33, wherein the method further includes coupling a bit line to another [first] gate of the dual-gate transistor in each inverter.

37. (Twice Amended) A method for forming a sense amplifier, comprising:

forming and cross coupling a pair of inverters, wherein forming and cross coupling each inverter includes:

forming a first transistor of a first conductivity type;

forming a dual-gate transistor of a second conductivity type, wherein forming the dual-gate transistor includes coupling the drain region for the dual-gate transistor to a drain region of the first transistor in each inverter, directly coupling the drain region for the dual-gate transistor in each inverter to a gate of the first transistor of the first conductivity type in the other inverter and to a gate of the dual-gate transistor of the second conductivity type in the other inverter;

coupling a bit line to a [first] gate of the dual-gate transistor in each inverter; and

coupling an output transmission line to the drain region of the first transistor and to the drain region of the dual-gate transistor in each inverter.

40. (Twice Amended) A method for operating a sense amplifier, comprising:

equilibrating a first and second bit line, wherein the first bit line is coupled to a first gate of a dual-gate transistor in a first inverter in the sense amplifier and the second bit lines is coupled to a first gate of a dual-gate transistor in a second inverter in the sense amplifier;

discharging a memory cell onto the first bit line, wherein discharging a memory cell onto the first bit line drives a signal from a drain region for the first inverter directly to a gate of a PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

providing a feedback from a drain region for the second inverter to a gate of a PMOS transistor and a second gate of a dual-gate transistor in the first inverter.

44. (Twice Amended) A method for operating a sense amplifier, comprising:

providing a first bit line signal to a first gate of a dual-gate transistor in a first inverter of the sense amplifier;

providing a second bit line signal to a first gate of a dual-gate transistor in a second inverter of the sense amplifier

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors drives a signal directly from a drain region for the first inverter to a gate of a

PMOS transistor and to a second gate of a dual-gate transistor in the second inverter; and

wherein providing the first and the second bit line signals to the first gates of the dual-gate transistors isolates the bit line capacitances from a first and second output node on the sense amplifier.

45. (Twice Amended) A method for operating a sense amplifier, comprising:

providing an input signal from a bit line to a first gate of a dual-gate transistor in a first inverter of the sense amplifier

wherein providing the input signal from the bit line to the first gate of the dual-gate transistor in the first inverter of the sense amplifier drives a signal directly from a drain region for the first inverter to a gate of a PMOS transistor and to a gate of a dual-gate transistor in a second inverter; and

wherein providing the input signal to the first gate of the dual-gate transistor isolates the bit line capacitance from an output node on the sense amplifier.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on March 22, 2001, and the references cited therewith.

Claims 1-2, 4, 10-11, 17, 23, 29, 32, 33, 35, 37, 40, 44, and 45 are amended, claims 3, 5, 12, 19, 25, 39 are canceled; as a result, claims 1-2, 4, 6-11, 13-18, 20-24, 26-38 and 40-45 are now pending in this application.